

Introduction

Thank you for participating in the Virtex[®]-7 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in [Table 1](#).

Table 1: Devices Affected by These Errata

Product Family	Device	JTAG ID (revision code)	Packages	Speed Grades	Junction Temperature Range
Virtex-7	XC7V2000T CES	2	All	-1, -2	0°C to 85°C
	XC7V2000T CES9925				0°C to 100°C

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

Power

Static Current

The devices listed in [Table 1](#) can exhibit up to 25% higher static current on all supplies compared to the static current reported in XPE.

Design Tool Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.07 (or later) of Xilinx[®] Vivado[™] Design Suite 2012.4 (or later) available at <http://www.xilinx.com/support/download/>.
- See Virtex-7 FPGA [Answer Record 52072](#) for the most current known issues and work-arounds for Xilinx Design Tools.

Traceability

[Figure 1](#) shows an example device top mark for the devices listed in [Table 1](#).

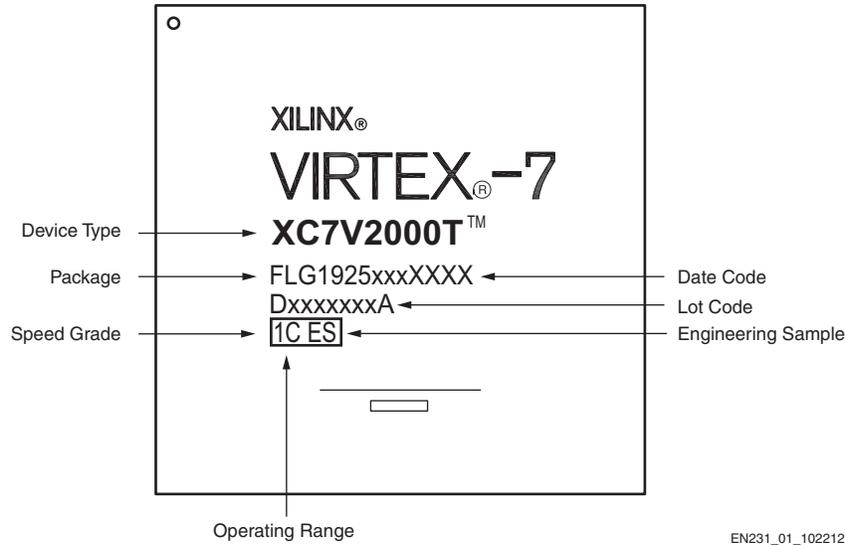


Figure 1: Example Device Top Mark

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact/index.htm>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/25/12	1.0	Initial Xilinx release.
02/12/13	1.1	Updated Design Tool Requirements .

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